PATENT APPLICATION

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AMENDMENT

Amendment to Claims

Please add the following claims as shown below.

~~7. (Newly added) An apparatus, comprising:~~

a static random access memory;

a processor coupled to the static random access memory;

a voltage regulator adapted to provide at least two voltage potential levels to at least a portion of the processor; and

wherein the processor is adapted to adjust the voltage potential level provided by the voltage regulator depending on the operational load of the ~~processor.~~

8 (Newly added) The apparatus of claim 7, wherein the voltage regulator is adapted to provide an idle voltage potential level and a peak voltage level.

~~9. (Newly added) The apparatus of claim 7, further comprising a state machine adapted to determine the operational load of the processor.~~

10 (Newly added) The apparatus of claim 9, wherein the state machine is further adapted to determine a minimum voltage potential level at which the processor can operate.

11 (Newly added) The apparatus of claim 7, further comprising a clock signal generator adapted to provide a clock signal of at least two frequencies.

~~12. (Newly added) A method comprising:~~

determining an instruction mix of a processor;

determining a frequency at which the processor may operate given the instruction mix; and

determining a voltage potential level corresponding to the frequency; and

providing at least a portion of a processor with the frequency and voltage potential level.

13. (Newly added) The method of claim 12, further comprising changing the frequency and voltage potential level in response to a change in the instruction mix of the processor.

14. (Newly added) A method of operating a processor, comprising:

adjusting the voltage potential level provided to at least a portion of the processor based on the instruction mix executed by the processor.

15. (Newly added) The method of claim 14, further comprising determining an operational frequency based on the instruction mix executed by the processor.

16. (Newly added) The method of claim 15, further comprising adjusting the operational frequency after adjusting the voltage potential level.

17. (Newly added) An article comprising: a storage medium having stored thereon instructions, that, when executed by a computing platform, results in:

adjusting the voltage potential level provided to at least a portion of the computing platform based on the instruction mix executed by the computing platform.

18. (Newly added) The article of claim 17, wherein the instructions, when executed, further result in determining a preferred operational frequency based on the instruction mix executed by the computing platform.

19. (Newly added) The article of claim 17, wherein the instructions, when executed, further result in computing platform executing the instruction mix at peak performance.

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20. (Newly added) The article of claim 17, wherein the article further comprises a static random access memory device and the computing platform is coupled to the static random access memory.

21. (Newly added) The article of claim 20, wherein the static random access memory is adapted to store the instructions to be executed by the computing platform.